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10EC45

Fourth Semester B.E. Degree Examination, December 2012
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Write switch level description in VHDL for the inverter circuit with nmos and pmos. Explain the advantages of this type description over the other types. **(08 Marks)**

b. Write the result of all shift and rotate operations in VHDL after applying them to a 7-bit vector A = 1001010 for one position. **(06 Marks)**

c. Explain verilog data types. **(06 Marks)**

2 a. Design 2 × 2 unsigned combinational array multiplier and write the VHDL code for the same. **(08 Marks)**

b. Draw the block diagram of a 3-bit carry-look ahead adder and write data flow description for its Boolean functions in verilog. **(08 Marks)**

c. Explain signal declaration and assignment with examples. **(04 Marks)**

3 a. Write the behavioural description for a half adder using verilog. **(04 Marks)**

b. Write the VHDL description for SR flip-flop using case statement and variable declaration. **(06 Marks)**

c. Explain Booth algorithm with flow chart. Write VHDL description to multiply two 4-bit numbers -5 and 7. **(10 Marks)**

4 a. Write gate level diagram and verilog structural description for D-latch. **(08 Marks)**

b. What is binding? Discuss binding between.
   i) Entity and architecture.
   ii) Library and component. **(08 Marks)**

c. What are the advantages of HDL structural description? **(04 Marks)**

PART – B

5 a. Write a VHDL function to find the greater of two signed numbers. **(06 Marks)**

b. Write HDL description to convert signed binary to the integer using task. **(08 Marks)**

c. What is the significance of procedure, task and function? Differentiate between them. **(06 Marks)**

6 a. Describe the development of HDL code for an arithmetic logic unit and write the verilog code for 16-bit ALU to perform 8 operations. **(08 Marks)**

b. Write the block diagram and function table of a 3SRAM. Using this write a verilog description for 16 × 8 SRAM. **(08 Marks)**

c. How to attach a package to the VHDL module? Explain with example. **(04 Marks)**

7 a. Write mixed language description of a JK flip-flop with clear, invoking VHDL entity from verilog module. **(08 Marks)**

b. Describe full adder using two half adder invoking verilog module from VHDL entity. **(08 Marks)**

c. Explain the necessity of mixed language description. **(04 Marks)**

8 a. What is synthesis? With a neat flow chart, explain the steps involved in a synthesis process. **(06 Marks)**

b. Design gate level synthesis and write VHDL description for the information given below:

Inputs		Output
a	b	z
00	0 – 7	z = b
01	0 – 7	z = b + 4
10	0 – 7	z = b/2
11	x x	z = 15
x x	8 – 15	z = 15

(14 Marks)

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